Report from the 'Silicon Upgrade Task Force'

Fermilab PAC Meeting
June 16-22, 2001

Marcel Demarteau
Fermilab

For the task force:

William Wester, Jeff Spalding, Petros Rapidis, Ron Lipton,
Joe Incandela, Brenna Flaugher*, Marcel Demarteau*

PAC Request

- Better understanding of commonality between the two Run2b silicon detector projects
- Director for Research set up 'Silicon Upgrade Task Force', May 4, '01
  - Membership:
    William Wester, Jeff Spalding, Petros Rapidis, Ron Lipton, Joe Incandela, Brenna Flaugher*, Marcel Demarteau* (* = co-chair)
  - Charge:

    " … to review the designs of the CDF and DØ Run IIb silicon detector designs and to recommend common solutions to common problems wherever appropriate. It is expected that other experts associated with the silicon upgrade will be asked to participate in the various discussions of the Task Force.

    The Task Force should also make suggestions for common design studies that should be undertaken and comment on priority R&D efforts that should be started early."
  - Consulted with:
    Nicola Bacchetta, Bill Cooper, Regina Demina, Jim Fast, Mike Hrycyk, Marvin Johnson, Hans Jostlein, Rich Partridge, Ray Yarema, Tom and Sergio Zimmerman, …
- At the same time a 'cost review' was undertaken (J. Cooper)

Task Force

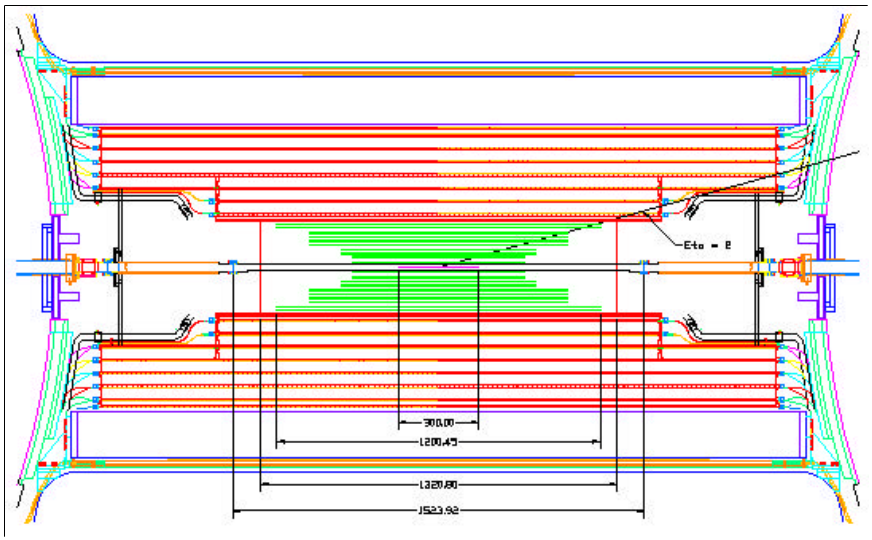
- First meeting May 7, 2001
- Series of meetings with task force and experts from projects
- Very limited amount of time available to discuss in depth with all parties
- Some findings on commonality will be presented
- In general,
  - Overall agreement that these meetings are very useful
  - Given that there are major areas of common interest it is highly desirable to have a continuity of exchange between projects

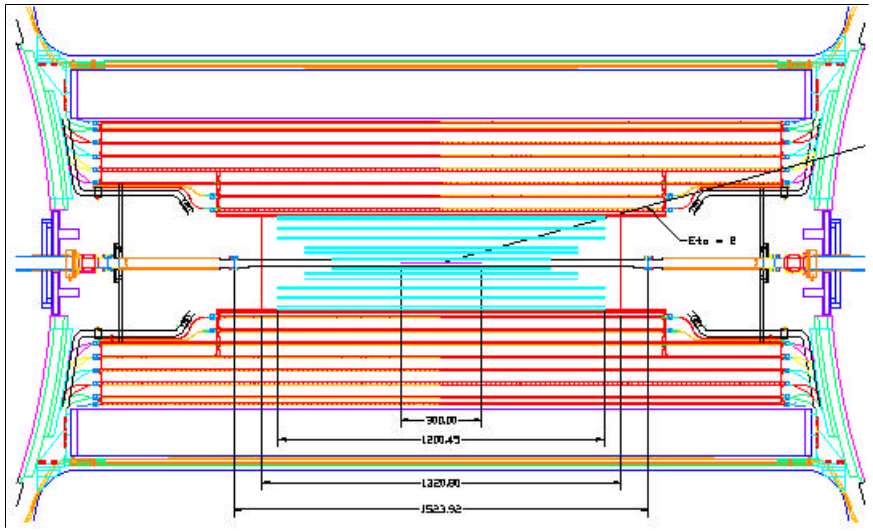
Outline

- Intrinsic differences between the two experiments
- Focus on commonality within each experiment's boundary conditions, working from inside out, with recommendations:
  - Luminous region
  - Beampipe
  - Structural support
  - Electronics
  - Tracker design
  - ...
- General Observations
- Summary and Conclusions

Presented at last PAC

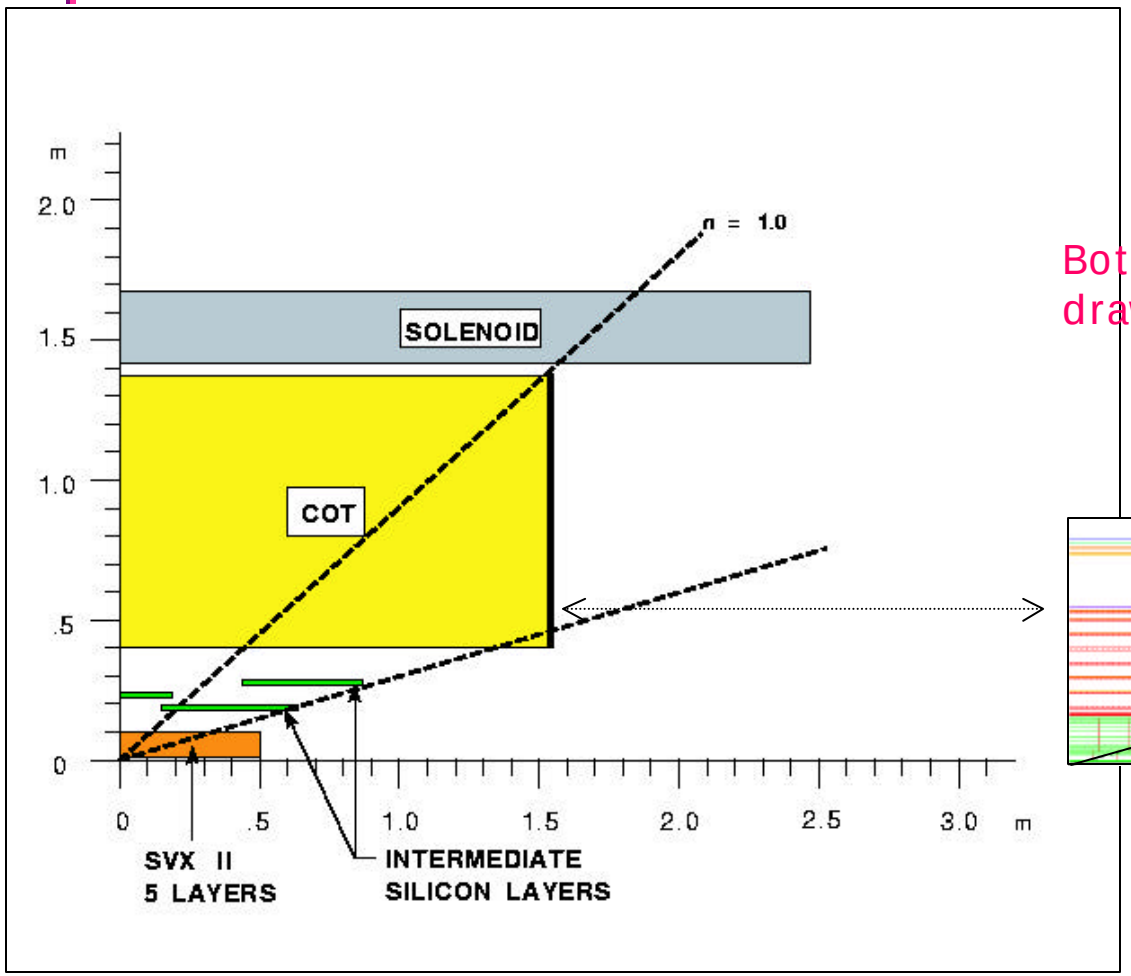
- Taken the silicon tracker designs as presented at the last PAC by both projects and drawn inside the DØ detector volume



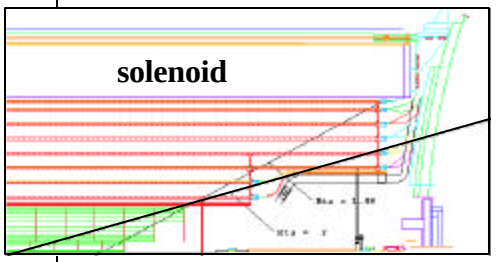


- But, …

CDF and DØ Central Tracking Volumes



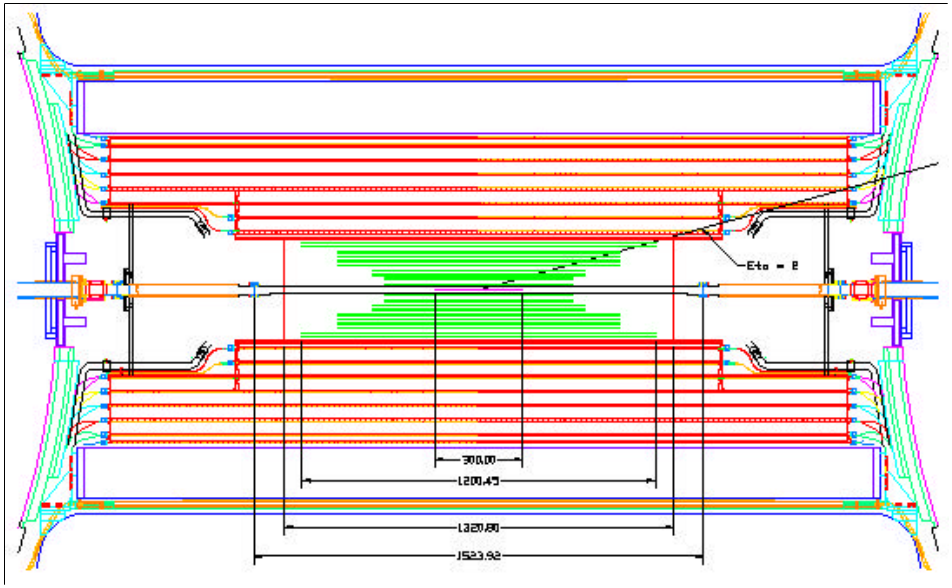
Both tracking volumes drawn to scale



η=2.0

- CDF: $R_{tracking\ volume}$ = 137 cm
- DØ: $R_{tracking\ volume}$ = 55 cm

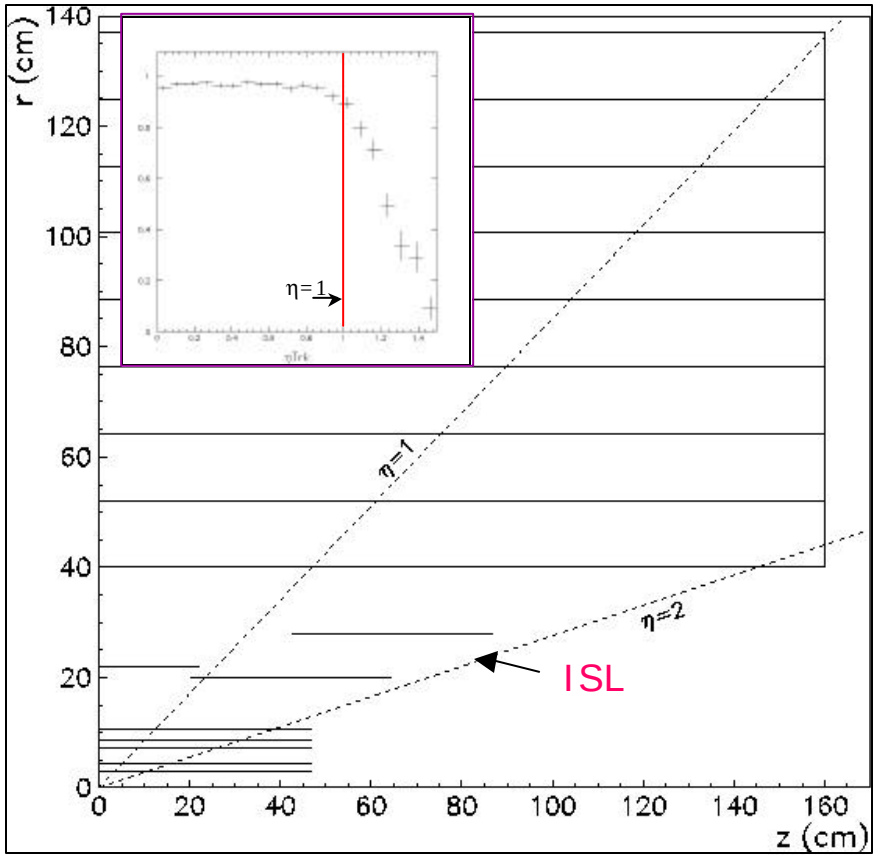
DØ Boundary Conditions



- Silicon tracker to be installed within existing fiber tracker, with inner radius of 180 mm
- Fiber tracker has full coverage up to $|\eta| < 1.6$
- Silicon stand-alone tracking up to $|\eta| < 2.0$

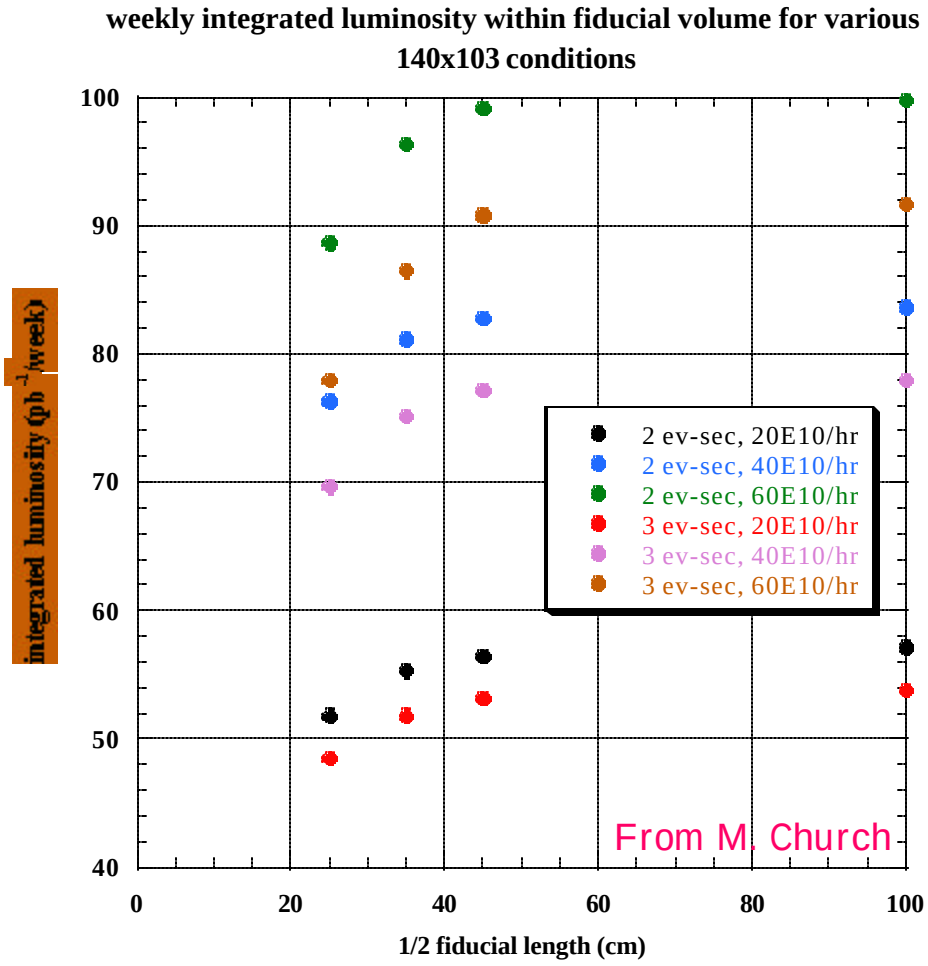
- Installation will occur in the collision hall
  - Installation in the Assembly Hall would add at least 3 months to the shutdown plus substantial risk
  - Thus, maximum length of device is 130 cm
    - Intercryostat gap is 39”
  - There is no room for off-board (outside tracking volume) electronics; hybrids have to be mounted in-board for the outer (longer) layers
  - Layer 0 and 1 will have off-board electronics

CDF Boundary Conditions



- COT has full coverage up to $|\eta| < 1.0$, with rapidly falling acceptance
- Silicon tracker installed within existing ISL, with inner radius of 180 mm
- Silicon stand-alone tracking in the region $1.0 < |\eta| < 2.0$ to recover from loss of COT tracking
  - Drive towards longer coverage in z
- CDF will retain ISL with two silicon layers at R=210, 290 mm
  - Combined with 2 ISL layers can do pattern recognition with only outer layers of Run2b detector
- No installation constraint on length of detector
  - Off-board electronics pursued for all layers
  - Proposed cooling implementation is different

Luminous Region



Longit. Emit. (eV sec)	Stack. Rate (E10/hr)	L/2 @ 90 % (cm)	Fract. Int. Lum (L/2 = 35 cm)	Fract Int. Lum (L/2 = 40 cm)
2	60	25	96%	98%
3	60	30	94%	97%
2	40	24	96%	98%
3	40	25	96%	97%
2	20	23	96%	98%
3	20	25	96%	97%

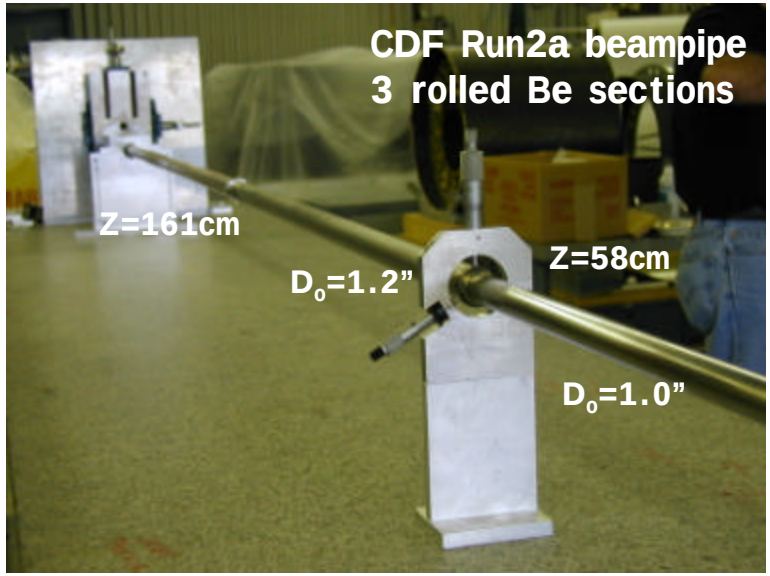
» Assumptions
- $\beta^* = 35$ cm
- Trans. $\varepsilon = 20/15\ \pi$.mm.mrad
- 0.5 crossing angle 136 μrad

- Address uncertainty on evolution of beam size over the course of a store
  - Coverage of inner layers of 80cm results in loss of ~3% of integrated luminosity
  - Assumed beam crossing centered at z=0; no uncertainties folded in
  - With uncertainties and L/2 = 40cm loss of more than 5% ?

Both experiments using the same information for their baseline design

Beampipe

- Be Beampipe has very long delivery time
  - 32 weeks for one beampipe and 46 weeks for two beampipes
  - Caveat: experience tells us that there are normally substantial delays
- Both experiments are considering drilled beampipes
  - 1" diameter: 0.8m, 500 μ wall thickness; 1.1m, 800 μ wall thickness (linear)
  - 1.5" diameter: maximum length 46" (117 cm), 500 μ wall thickness
- Length constraints
  - DØ max length 60"
    - » Installation in collision hall
    - » Flanges at the ends
  - CDF no length constraint
    - » May wish to push flanges further out
- Radius:
  - Experience with Lyr00 can be a guide
    - » In time?



- Recommendations:
  - Projects should settle on inner Radius and length of inner section of beampipe as quickly as possible and pursue joint purchase
  - Submit joint PO as quickly as possible

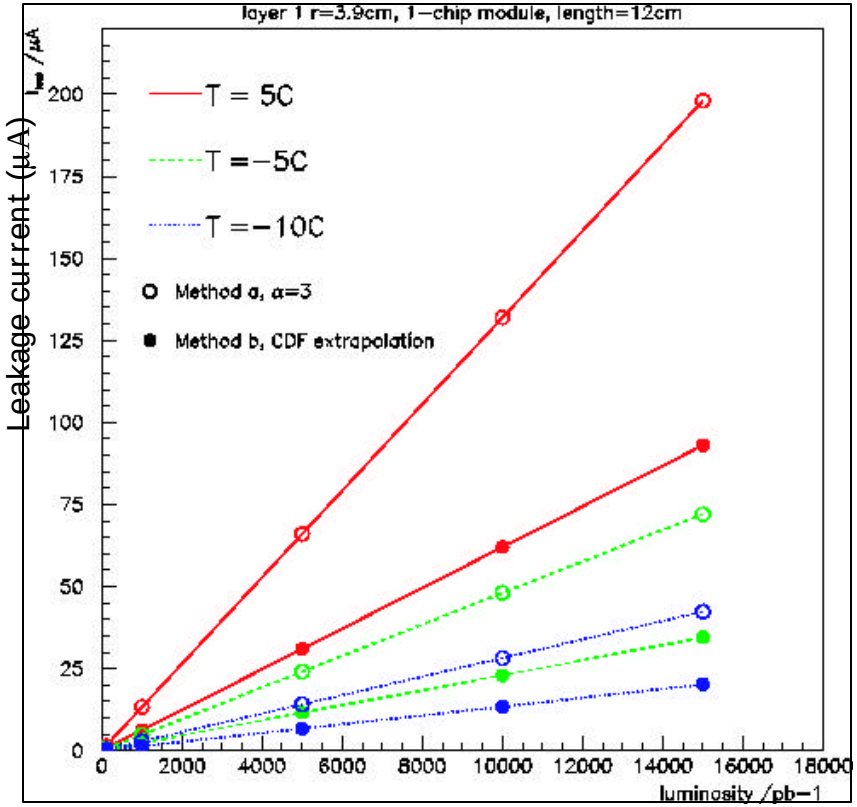
Silicon

- To first order complete commonality
  - Projects need of the order of 4500 sensors (at April PAC: 1656 + 2394)
  - Limited number of qualified vendors
  - Joint order provides additional leverage
- Actual sensor layout will be determined by physics requirements of silicon detectors embedded within their subsystems
  - Length, masks, pitch, stereo angle, …
    - » Not a cost driver anyway given total sensor cost of ~3.7M$
  - Highly unlikely that there will be a large overlap in the masks
    - » Possibly common sensor for inner layers
- There's a lot to be gained by a joint, coordinated approach for sensors
  - Quality management
    - » Database, probing
    - » Irradiation (Cleo)
  - Contract leverage
- Likely that the experiments will use the same vendors for a substantial fraction of their detector orders.

- Recommendation:
  - Projects should cooperate in vendor contacts
  - Projects should share technical and testing information and ensure that there are no conflicts in delivery schedules

Cooling

- Common to both projects (ISL on separate chiller)
  - Heat Load
    - ~30 Watts ambient
    - ~25 Watts at 15 fb^{-1} at innermost layer (T= -5 ^{o}C)
  - Desired Si Temp. –10 ^{o}C to –5 ^{o}C
  - Current system 70-30 water-glycol mix
    - T_{clnt} = -10 ^{o}C for CDF / DØ
    - Cannot go lower in T, viscosity
  - No wetted Be in either project
    - Different coolants possible
  - Need consensus on
    - Radius
    - Acceptable upper T for Si



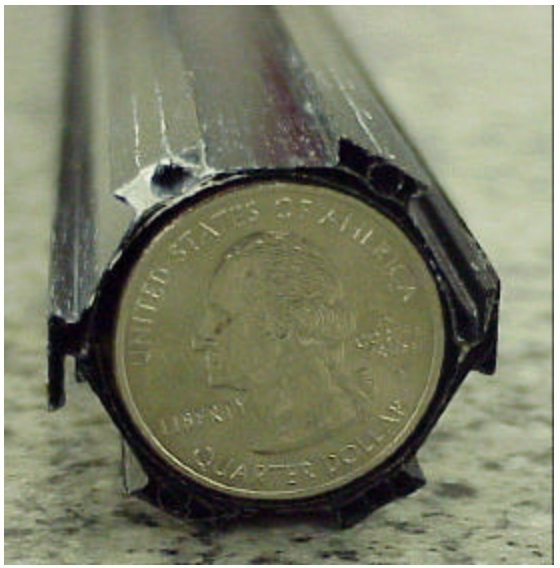
$\Phi \sim R^{-1.7}$

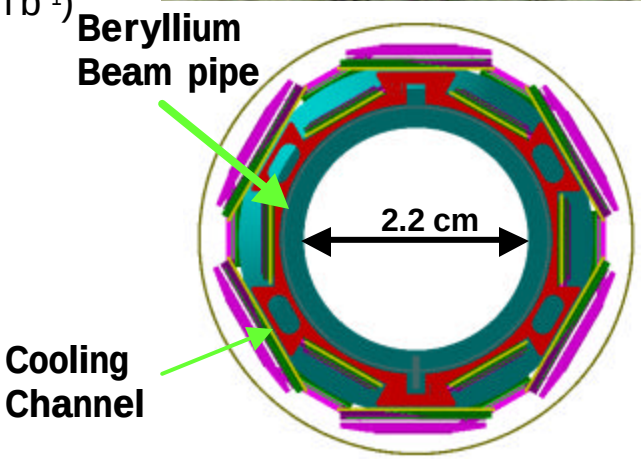
$I_{leak} \sim T^2 \exp(-E_g / (2 k_B T))$

- Recommendation:
  - Use of common coolant for both projects would minimize R&D time
  - Build into existing cooling system

Support Structures: Inner Layers

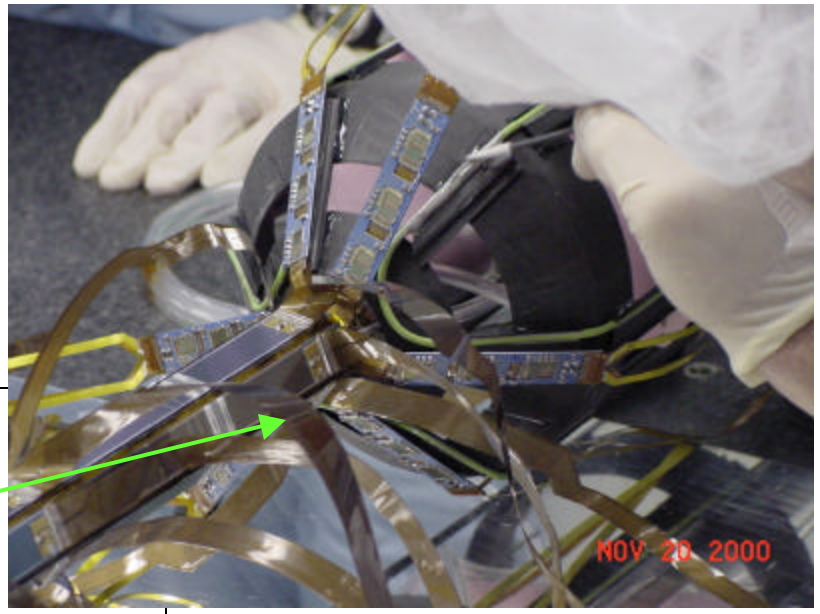
- Both projects will have innermost C-fi layers surrounding the beampipe
- Both projects will have off-board electronics for inner layers
- Large areas of commonality
- Support structures
  - Difficult to build
    - » High precision
    - » Integrated cooling
    - » High thermal conductivity
    - » High stiffness
      - Recall: Liverpool ~ 1 year to build Lyr 00 Cf support
      - Si needs to be at lower T for 2b
      - Lyr00 warmest –2 °C (4 °C) at begin run (at 5 fb^{-1})
    - » Large parameter space
      - Fibers, epoxies, lay-up, …
  - Many more structures needed
    - » Layers 0, 1 for DØ
    - » Layer 0, 1, 2 for CDF

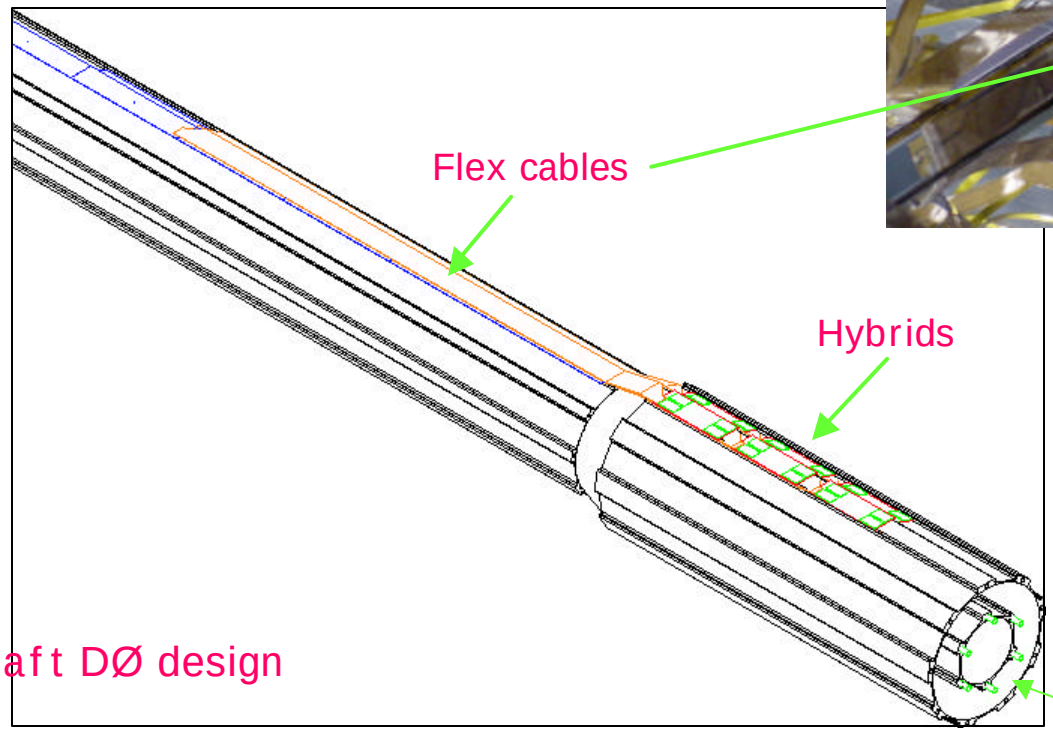




Support Structures: Inner Layers

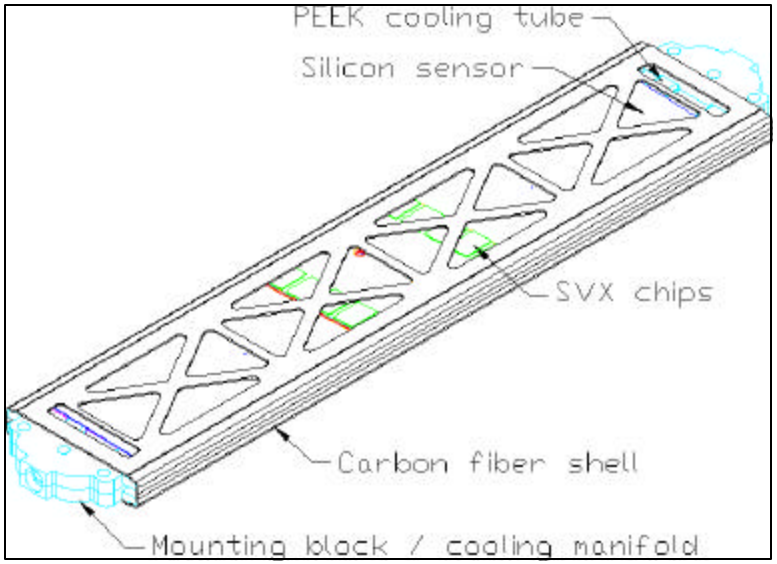
- Electronics are off board
  - Separate support structures for hybrids
  - Independent cooling lines
- CDF's intent is to have electronics off board for all layers

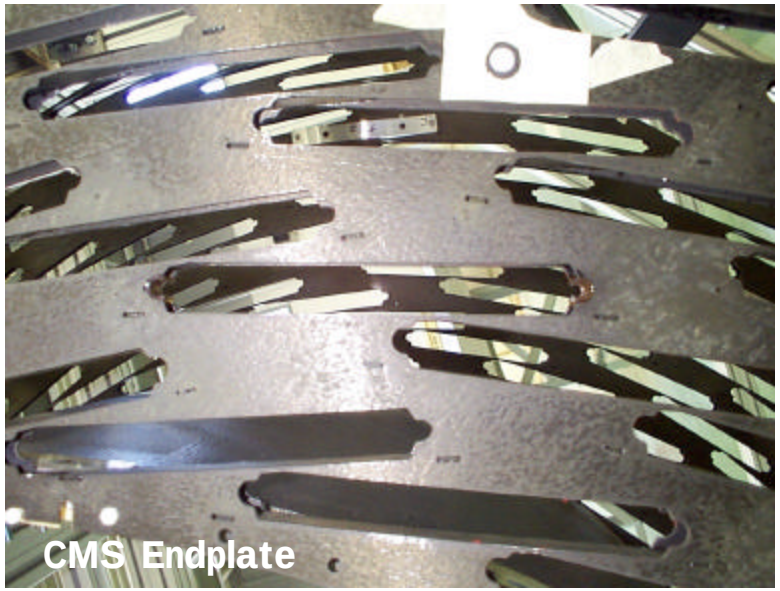




Support Structures: Outer Layers

- Branching Point
  - CDF: off board electronics
  - DØ: on board electronics
  - ⇨ Different module design and consequently different stave design
- Conceptual Designs:
  - Similarities
    - » C-fi support cylinders
    - » Sensors on either side within module
    - » Staves mounted on C-fi cylinders
    - » Precision plates inside and at the ends
    - » Alignment of cylinders
  - Differences
    - » DØ active cooling of staves
      - On-board electronics requires cooling chips and Si
    - » CDF separate cooling of hybrids
      - Passive cooling of Si





Support Structures

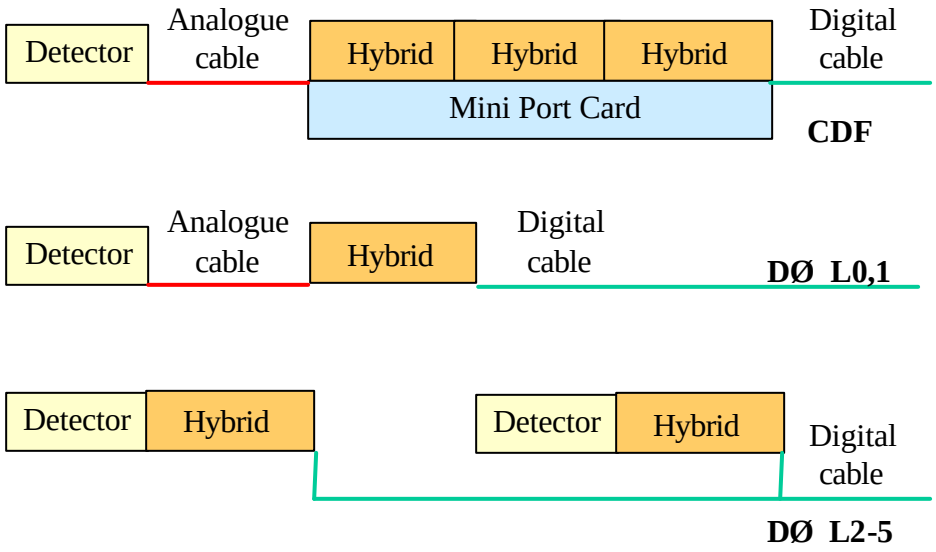
- Commonality:
  - Inner layers:
    - A lot of areas are common between the two projects
  - Outer layers:
    - Natural branching point due to hybrids
  - Methods and technologies being considered are completely in common between the two projects (common R&D already started)
  - From previous experiences, long lead times before converging on acceptable design

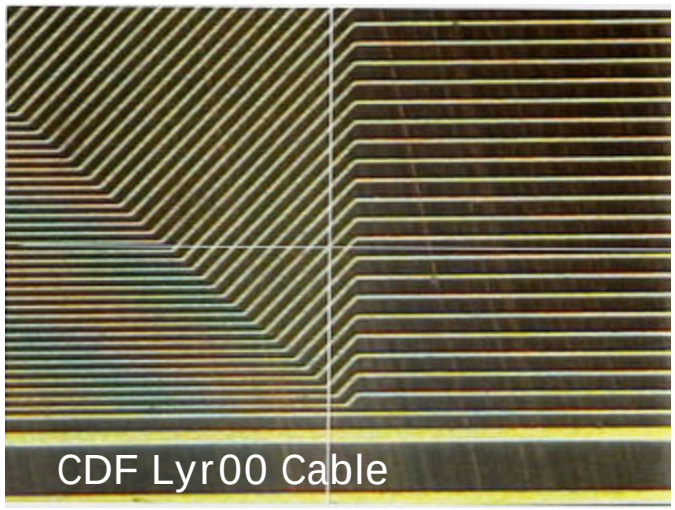
- Recommendation:
  - R&D efforts on support structures and prototyping should commence as quickly as possible
  - Exchange of ideas and learning experiences of the projects should occur regularly in a well defined forum

Flex Cables

- Low mass, fine pitch cables to bring analogue signals outside of tracking volume
  - Large number of cables needed
    - » CDF: 1776 (2664)
    - » DØ: 240 (360)
  - Technically challenging
    - » Feature size <50μm
    - » Lyr00 cables 'handcrafted' by CERN
    - » DØ vlpc cables: difficult to get reliable cables
  - Very few vendors
    - » CDF: Keycom (Japan)
    - » DØ: Dyconex (Switzerland) (as experimental run)

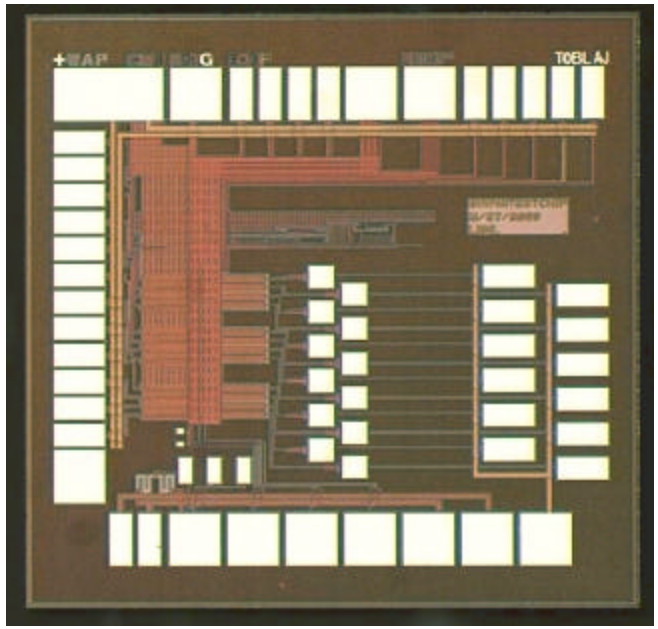
- Recommendation:
  - Experiments should work together on qualifying cables and (alternate) vendors





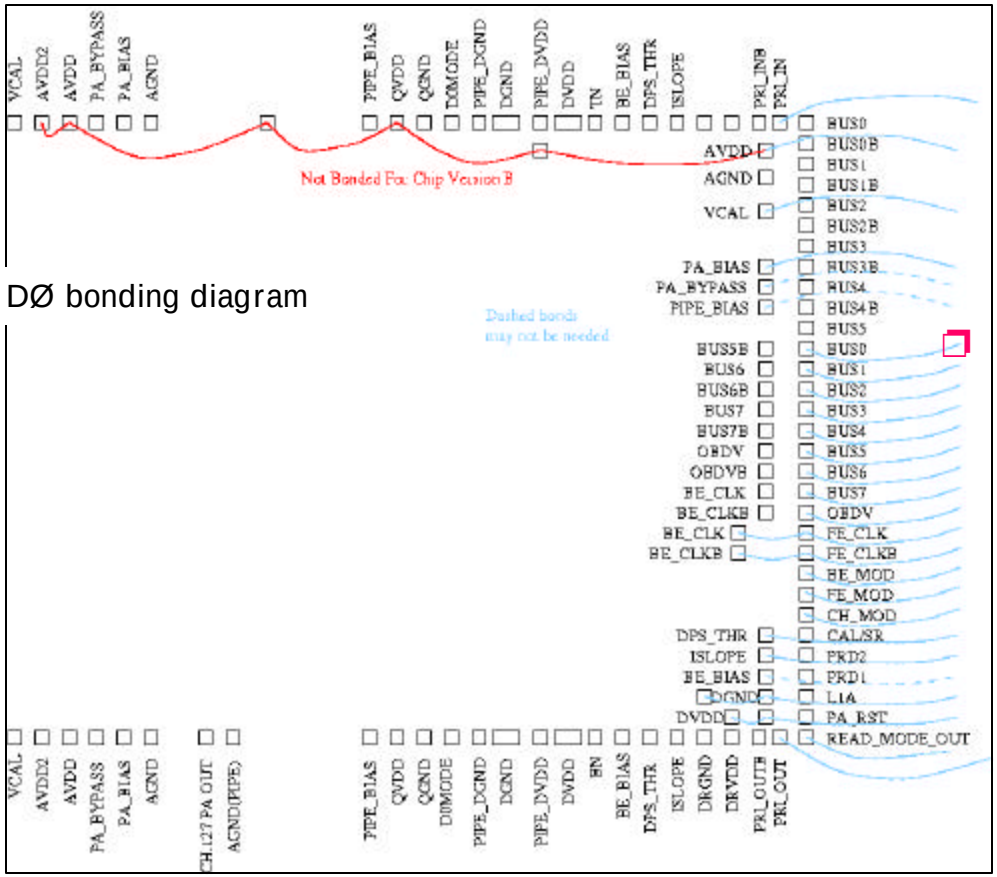
SVX4 Chip

- Nov '00 decision to employ common readout chip for CDF and DØ
  - SVX4 in deep sub-micron, 0.25 μm technology, intrinsically rad-hard
    - Brand new chip with own personality/features
  - Commercial foundries
- Joint effort between FNAL (pipeline), LBNL (front-end, overall integration) and Padova (data sparsification)
- Analogue test chip submitted to MOSIS 11/25/00, received early March '01
  - 12 pre-amp test chips received, showed feasibility in 0.25 μm technology
    - Linearity < 1%
    - Gain 1.25 mV/fC (low due to incorrect C_F)
    - Enc = 1750 e for 40pF load for test chip w/o double-correlated sample
- Design Review at LBL April 23-24, '01
  - Review was a bit early
  - Recommendations
    - Critical circuit blocks should be implemented in test chip submissions (pre-amp, FIFO, ...)
    - Test chips evaluated before full chip submission



SVX4 Chip: Boundary Conditions

- CDF (SVX3 mode)
  - Chip operates in deadtime less mode
  - Differential signals
  - Power, bias, bypassing along top and bottom edge of chip



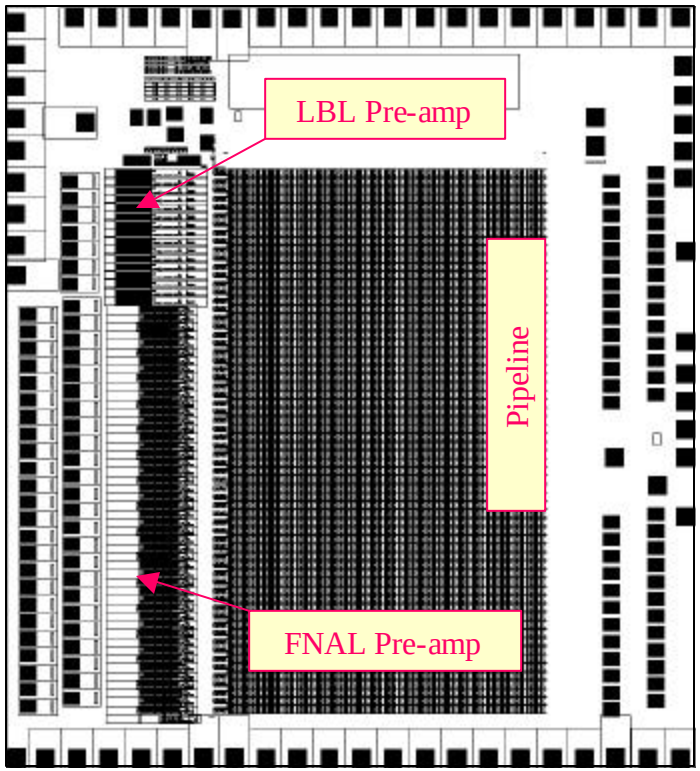
DØ bonding diagram

- DØ (SVX2 mode)
  - Uses single clock for FE and BE, incurs deadtime
  - Signals single-ended
    - Internal logic can be used to program chip for either mode
  - Sensor pitch of 55 or 60μm (nearly) prohibits edge chip connections
  - Power, biasing and bypassing off the back-end of the chip

- Due to number of separate power bonds and limited space at backend
  - On-chip bypassing suggested
    - Capacitor array distributed under pipeline for AVDD to substrate
    - Analogue power bus lines needed from BE to FE; run over digital buses
      - Some concern it may cause problems in deadtime-less mode

SVX4 Chip

- Test chip submitted to MOSIS 06/04/01
  - 16 channels LBL design preamp + pipeline
  - 48 channels FNAL design preamp + pipeline
    - » Common bias preamp+pipeline as in SVX3
    - » 12 different input transistor sizes used to optimize noise
  - Submission has on-chip bypassing
  - Due to ship July 26



- Current schedule:
  - Full size chip submission in September; two chip versions:
    - » Version A (CDF):
      - External bypassing
      - Buses for power and bias not connected to back-end
      - Redundant pads for power routing
    - » Version B (on-chip bypassing, DØ):
      - Power bused internally
      - On chip bypassing under pipeline array
      - Pads only on backend of chip

SVX4 Chip

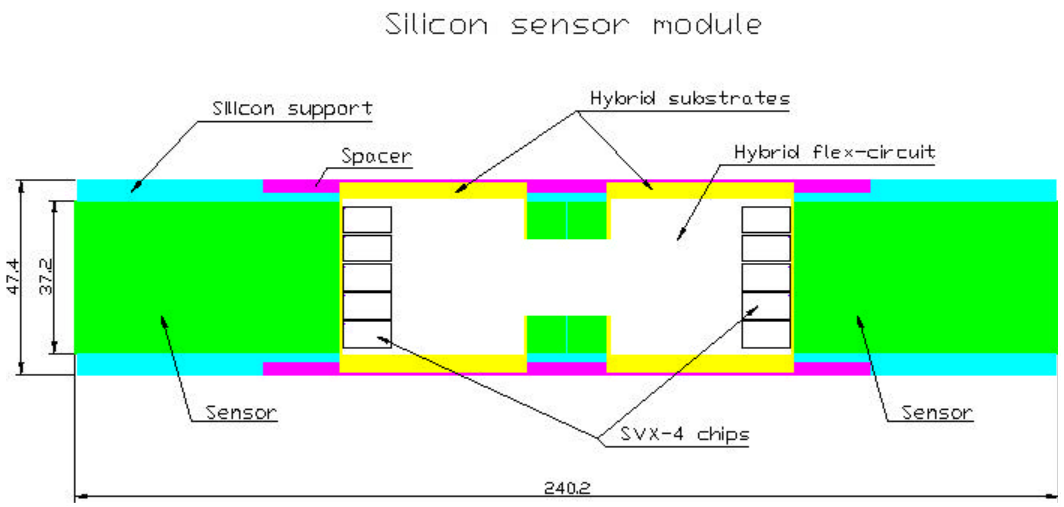
- Progress on chip of this complexity has been good;
  Need good coordination of work of various groups to maintain schedule

- Recommendations:
  - Pad frame layout and power busing should be finalized as quickly as possible
  - Clear set of criteria should be given for acceptance of various designs
  - Having a well performing first full chip, completely functional, should be the highest priority
  - Reiterate the recommendation of the review committee for test chip evaluation before full chip submission
  - Follow with full verification of design simulation (with changes if necessary) and external review before submission
  - Both projects should give highest priority to having one common chip and weigh potential small delays against project schedule; laboratory should endorse common chip.

Hybrids

- Branching point:
  - Different mode of operation of SVX chip
  - On board versus off board electronics
- Commonality may be limited to
  - Inner layers
  - Using same technology
    - » High density flexible interconnects laminated to substrate (Be)
    - » Ceramic hybrids (Al_2O_3 or BeO) w/ silkscreening and etching

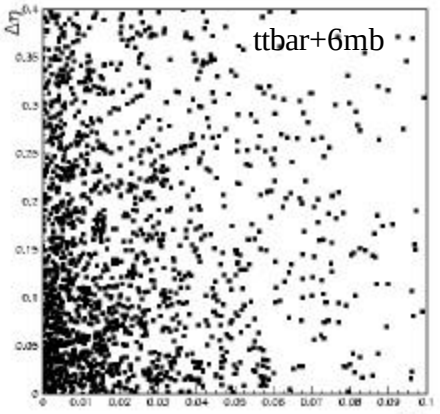
Material	X_0 (cm)
Be	35.3
BeO	13.3
Al_2O_3	7.3



- Recommendation:
  - Continue dialogue

Tracking

- Branching point:
  - CDF has two additional silicon layers, ISL
    - » Combine ISL layers with outer layers of Run2b detector for pattern recognition
    - » Considering 90-degree stereo
      - Improve b-tag purity for 2-track tags
      - Concern: Track overlaps, wrong hit selection, ghosts
      - Mitigated by:
        - » Smaller pitch, larger stereo angle in outer layers
        - » Provides better pointing to 90-degree stereo layer at fairly large radius where occupancy is low



Select Δϕ min → check Δη

  - DØ's emphasis on Rϕ-impact parameter resolution and pattern recognition
    - » Keeping all options open
- Both projects in the midst of occupancy, pattern recognition, physics studies to address:
  - Sensor length, ganging
  - Pattern recognition, ghosting, mistag rejection
  - Radial positioning of layers
  - Stereo angle, 90-degree stereo

Example Occupancy Study

- Fraction of tracks that have another track within 100 μm or 200 μm in R-ϕ for pp → WH → eν + bb for possible longitudinal readout segmentation (signal only)

DØ

	0	40	80	120	160	200	240	280	320	360	400	440	480	520	560	600
Layer 0		25		24		25		26		37						
Layer 1		13		11		11		14		26					< 100 μm	
Layer 2		7			8		7				11					
Layer 3		5			5		5				3					
Layer 4					4							4				
Layer 5					2							2				

	0	40	80	120	160	200	240	280	320	360	400	440	480	520	560	600
Layer 0		43		40		43		44		51						
Layer 1		23		22		21		24		36					< 200 μm	
Layer 2		12			12		14				16					
Layer 3		8			8		9				7					
Layer 4					6							9				
Layer 5					5							4				

- Occupancy numbers very high for inner layers
  - Highly inclined tracks makes it worse. May force larger radius, thinner Si
  - CDF L00 design studies indicate that at a radius of 1.4 cm, 33% of b-daughter tracks from ttbar share clusters with another track but 45% of these clusters can be split.

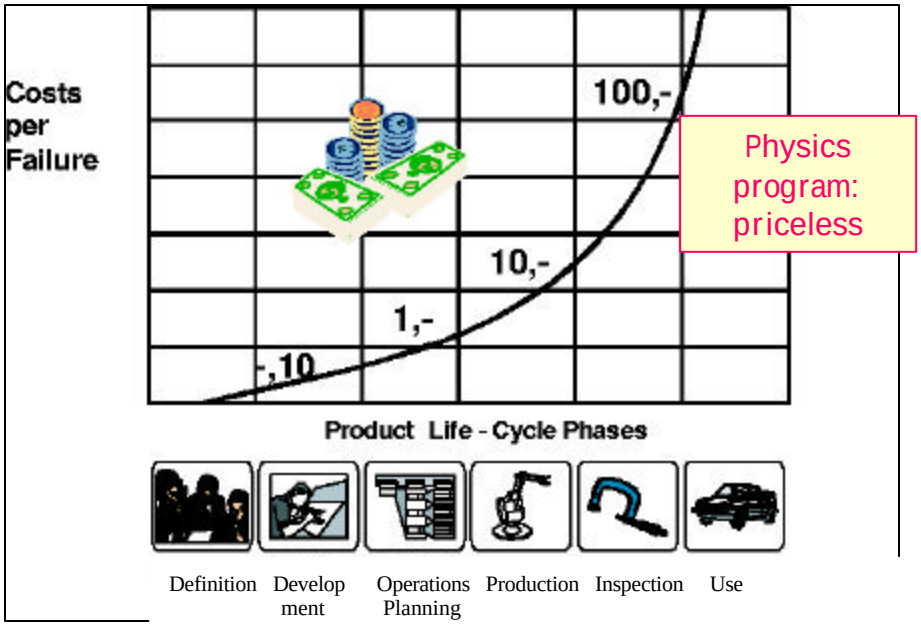
Tracking

- Collaborations are in the midst of detailed tracking studies
  - Pattern recognition
  - Occupancy studies
  - Charge sharing
  - Full simulations
- Too early to come to a conclusion on tracker layout.
  Collaborations should continue their discussions

Quality Management

- Best efforts for Run2a on
  - QC:
    - » Personnel stationed at Micron
  - QA:
    - » Database
    - » Regular feedback with vendor
- But, if you have 100 sensors and you need 100 sensors, there is not much of quality control
- Both CMS and ATLAS are setting up impressive procedures for QA & QC
  - Vendors are provided with Java scripts for database entry
  - "Baby sensors" included in processing batches, which will be irradiated

CERN QA Workshop, May '01



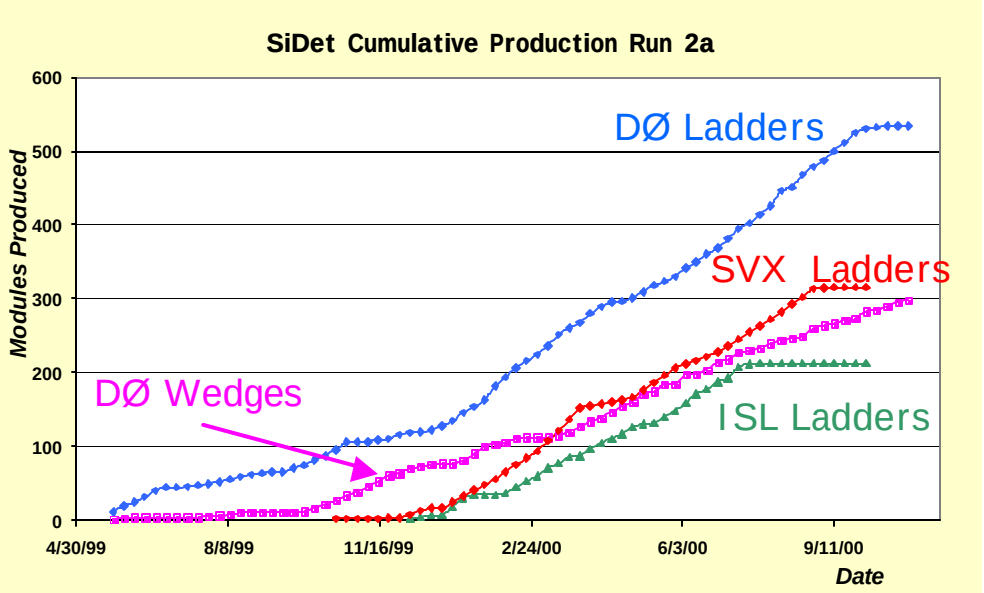
- Most defects introduced in early stages of 'product life-cycle'
- Ultimate price is that due to limited detector performance physics is out of reach

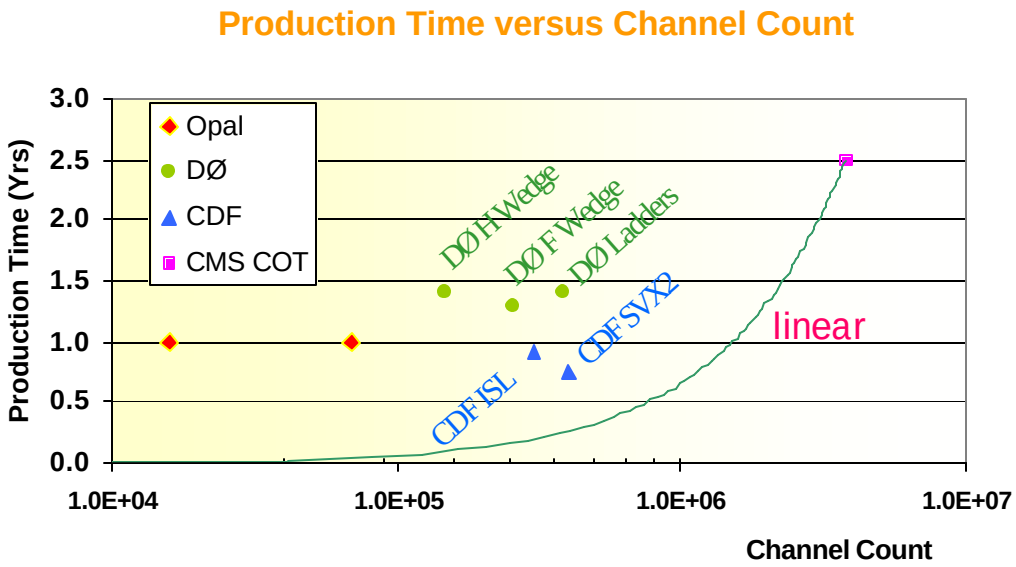
Quality Management

- Recommendation:
  - Given that both experiments will most likely use same the vendors, notably for silicon and flex cables, with central receiving location:
    - » Centralized, coordinated Quality Planning should start as soon as possible
    - » One approach for both experiments
    - » Support for common QA/QC tasks, like irradiation tests, should be an integral part of the planning and provided by SiDet
    - » Software efforts, like database development, should be supported by the Computing Division

Features of Production

- Actual production of ladders, modules, staves rather quick
- For devices with less than 1M channels, nearly a constant production rate
- Preproduction can vary wildly
  - R&D, engineering issues
  - Vendor issues
    - » Qualification
    - » Delivery
  - Prototyping
  - Testing
  - ...
- Given the short time scales for completion of these projects it is crucial that the projects are adequately supported





Resources

- Also common between the projects is that they rely heavily on Fermilab SiDet resources
- Silicon tasks are quite specific and have a long lead time
- Given the time scale on which detectors have to be completed, resources are inadequate
  - 2 CMM operators needed
  - 2 Mechanical engineers needed
  - Common R&D has started but needs adequate resources
    - » Thermally conductive materials and measurement equipment
  - ...

- Recommendation:
  - Resources within the laboratory should be reevaluated and realigned given the priorities of the physics program
  - Common projects should be adequately supported through SiDet

Summary and Conclusions

- Commonality in major areas between the two projects
- Although details will differ, common technology choices will lead to great benefits
- General consensus:
  - Discussions between collaborations and engineers were useful and should continue
  - Regular meetings should be held with projects
    - » Pursue common vendors, common purchase contracts
    - » Exchange ideas, exchange data on common projects
    - » Identify areas of collaboration
      - SVX4 testing
      - Sensor qualification and irradiation studies
      - Beampipe, Si and flex cable purchase contracts
      - C-fi support structures
      - ...
  - Common R&D projects and support coordinated by SiDet